# TMC2063

## Demonstration Board for the TMC22091 and TMC2490 Digital Video Encoders

## Features

- Parallel CCIR-656-format ECL input
- Multiple video formats
  NTSC, NTSC-EIA (Japan)
  PAL-B,G,I, PAL-M, PAL-N
- Composite and S-Video outputs
- Built-in test patterns
  Color bars – TMC22091
  Modulated ramp – TMC22091, TMC2490
- No external components required
- Serial interface to control TMC2490
- Master mode port to control TMC2490

## Applications

- Evaluation of TMC22091 and TMC2490 digital encoders
- System breadboarding
- Encoder control program development

## Description

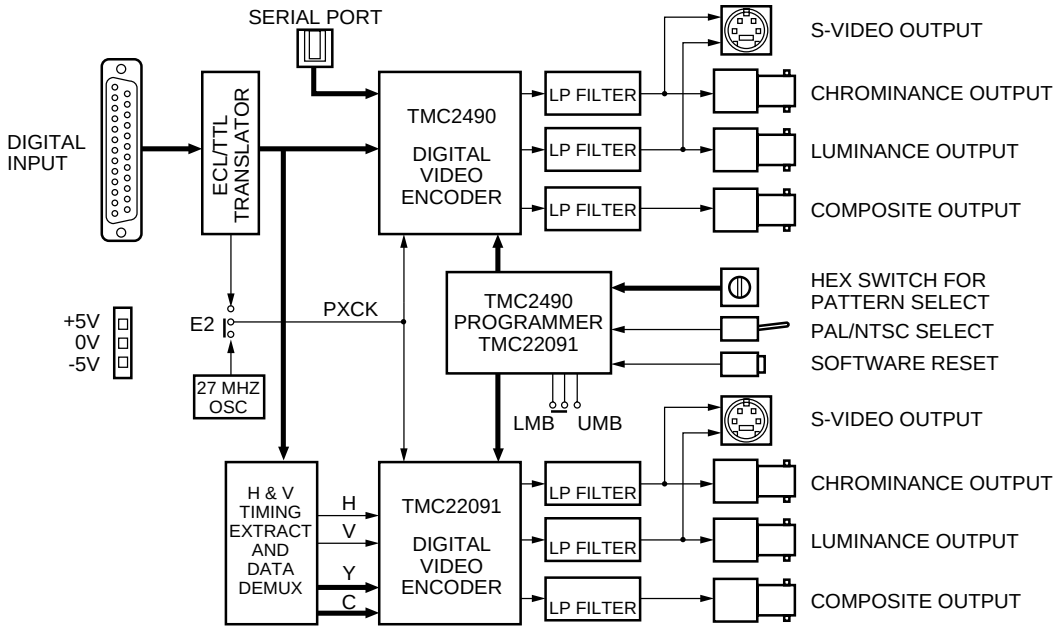
The TMC2063P7C encoder demonstration board converts 8-bit parallel digital component video, (CCIR Rec. 656 or ANSI/SMPTE 125M, a.k.a. “601”) into analog composite video using the TMC22091 and TMC2490 digital video encoders. The board supports multiple standards, operating in PAL, PAL-M, NTSC, and NTSC-EIA (zero setup) television formats.

A 27 MHz crystal oscillator is provided for cases where a CCIR-601 source is not available. When operated from the on-board oscillator, only the internally generated color bars and modulated ramp can be produced from the TMC22091.

The TMC2063 is designed to demonstrate the performance of the TMC22091 and TMC2490 Digital Video Encoders, while providing a convenient testbed for developing specific programming for the encoder and evaluating the resulting waveforms. It also offers an example of design practices that result in high-quality video performance.

The board supports multiple standards, operating in PAL, PAL-M, NTSC, and NTSC-EIA (zero setup) television formats. The data must be provided with the proper frame rate, but any supported 50Hz format may be produced with the supplied programs.

## Block Diagram



The board accepts 8-bit parallel digital component video, (CCIR Rec. 656 or SMPTE RP 125, a.k.a. "D1") at a standard D25 connector in differential ECL format and translates the data to TTL format. The TMC2490 accepts the multiplexed D1 data stream and internally strips the Timing Reference Signal (TRS) to produce the required horizontal and vertical references. The D1 data for the TMC22091 is externally processed to strip the Timing Reference Signal from the data stream to generate H&V Sync, and is demultiplexed to pass the digital video stream to the Encoder in a 16-bit 13.5 MHz format. The TMC2490 may also be operated in Master Mode by interfacing the Pixel Data (PD) bus through header JP1.

A simple EPROM-based programmer is provided, which downloads the selected configuration (one of 64) to the two digital Encoders when the reset button is pressed, through the parallel microprocessor interface. This EPROM holds both control register data and Color-Look-Up-Table (CLUT) patterns in 1K blocks. Sixteen pages are selected by a rotary switch, and additional switches are provided for selecting the required video standard.

The board operates from standard ±5V supplies. When used in stand-alone mode, only +5V is required.

## CCIR-601 Interface

The CCIR-601 data stream is terminated into differential ECL-to-TTL converters. The translated data is latched through U16 at a 27 MHz rate and then passed directly to the TMC2490, the YC demultiplexer, and the TRS decoder. The TMC2490 locks the internal state machines to the TRS words embedded in the D1 data stream. The horizontal state machine produces the control signals required to separate the CbYCr[Y] data and interpolate the CbCr color difference signals to the luminance sample rate. For the TMC22091, the luminance and chrominance data words are separated into two data streams termed Y and C, respectively, externally in the YC demultiplexer. This YC data goes directly into the TMC22091, which separates the C data stream into its two color difference signals and interpolates them to the same sample rate as Y data. This interpolation, as in the TMC2490, improves the horizontal color definition.

The TRS decoder extracts the field (F), vertical blanking (V), and horizontal blanking (H) information from the D1 data stream for use in the timing signal generation on the board. The TRS decoder also produces the pixel counter reset and the LDV signal for latching the YC data into the TMC22091.

## Master Mode Interface

A MASTER mode pixel data bus is available on header JP1. In the default slave mode, pins 25 and 26 are left unconnected. The PD port of the TMC2490 receives its input from the ECL to TTL slave interface. By connecting pins 25 and 26 the TMC2490 receives the pixel data (PD) from the header JP1. In addition, all synchronization pins are connected to JP1 which allows access to these pins when the TMC2490 operates in a MASTER mode.

## Horizontal and Vertical Timing for the TMC22091

The pixel counter (U3, U11, and U2) is decoded to produce the $\overline{\text{VHSYNC}}$ and PDC signals required by the TMC22091 in Slave Mode for horizontal synchronization. A 2x line rate clock, H/2_CLK, used in the $\overline{\text{VVSYNC}}$ generation, is also produced along with P_CLOCK and DATA_EN. P_CLOCK is used to clock the program counters and the DATA_EN signal used in the YC demultiplexing circuit.

A 4-bit counter embedded in U8 is started whenever V goes HIGH, which occurs at the beginning of each vertical blanking interval. This counter is clocked by H/2_CLK, which enables the $\overline{\text{VVSYNC}}$ pulse to be produced at the same time as the first vertical sync pulse in each field. The PGM output signal ensures that the software reset signal, RES_OUT, goes HIGH 15 half-line periods before the program counter starts.

## Software Reset

A software reset occurs whenever the pushbutton switch, S2, is depressed. The software reset is latched through U8 to ensure a known relationship between the internal pixel clock of the external PXCK clock in master mode. When S2 is depressed the internal state machines of the TMC22091 and TMC2490 are reset and the outputs are disabled. When S2 is released the program counter is started at the beginning of the next vertical blanking period, when a D1 input is provided, or immediately if the TMC22091 is being programmed to produce master mode test patterns. Software Reset is required after power-up and after each functional change.

## Programming the TMC22091 and TMC2490

A 12-bit counter (U1, U9, and U10) is used to produce the addresses used in programming the TMC22091 and TMC2490. U13 produces the required R/$\overline{\text{W}}$, A1:0, and $\overline{\text{CS}}$ signals for the TMC22091 while U17 produces the R/$\overline{\text{W}}$, ADR, and $\overline{\text{CS}}$ required by the TMC2490. The EPROM, U22, contains 32 different pages of setup data for NTSC and another 32 pages for PAL (selected via switch S3). Switch E4 selects between different flavors of NTSC and PAL operation. To ensure that the outputs of the programmable logic (U13 and U17) are correctly timed to transitions on the microprocessors data bus, they are addressed at four times the rate that U22 is addressed. The 16 pages of setup data are selected by the rotary switch S1, as shown in Table 1.

The TMC2490 produces an internal ramp pattern for rotary switch positions 0, 1, and 2 and encodes the D1 input data for positions 3 through F.

The programming of the encoder operation into each of the 64 memory pages by banks of 16 by video standard (Table 2) is entirely arbitrary: one could as easily assign CCIR-601 operation in the four supported formats to pages 0-3, and color bars to pages 4-7. The user is encouraged to replace the EPROM with one programmed with other formats of interest.

## On-Board Read-Only Memory

Table 3 shows the content format of the EPROM that holds the 64 pages of setup data. The encoder register contents are defined in the TMC22091/TMC22191 data sheet.

The TMC2490 produces an internal ramp pattern for rotary switch positions 0, 1, and 2 and encodes the D1 input data for postions 3 through F.

### Table 1. Operational Setups for the TMC2063

| Rotary Switch Position | TMC22091 Function | TMC2490 Function |
|---|---|---|
| 0 | Color bars test signal (8-bars) | Internal Test Ramp, Slave mode without PDC, Trad, VSync |
| 1 | Color bars test signal (9-bars) | Internal Test Ramp, Slave mode without PDC, Trad, VSync |
| 2 | Modulated ramp test signal | Internal Test Ramp, Slave mode without PDC, Trad, VSync |
| 3 | Encodes CCIR-601 input data (normal operation) | Encodes CCIR-601 input data in Slave Mode with Timing - PDC, Trad, Vsync |
| 4 | Subcarrier data limited to 28-bit resolution | Encodes CCIR-601 input data in Slave Mode with Timing CBSEL and Field ID |
| 5 | Subcarrier data limited to 24-bit resolution | Encodes CCIR-601 input data in Slave Mode with Timing - PDC, Trad, Vsync Chroma Bandwidth limited to 650 kHz |
| 6 | Luminance data limited to 6-bit resolution | Encodes CCIR-601 input data in Slave Mode with Timing - PDC, Trad, Vsync with YCDelay Active |
| 7 | Chrominance data limited to 6-bit resolution | Same as Rotary Switch Position 3 |
| 8 | Luminance and chrominance data limited to 6-bit resolution | Same as Rotary Switch Position 3 |
| 9 | Inverted luminance data | Same as Rotary Switch Position 3 |
| A | Inverted luminance data and 180° phase shift to chrominance | Same as Rotary Switch Position 3 |
| B | Chrominance data set to constant value in UV CLUTs | Same as Rotary Switch Position 3 |
| C | Color burst phase advanced 10° | Same as Rotary Switch Position 3 |
| D | Color burst phase retarded 10° | Same as Rotary Switch Position 3 |
| E | Reduced active video line length | Same as Rotary Switch Position 3 |
| F | Black burst (NTSC includes pedestal) | Same as Rotary Switch Position 3 |

**Table 2. Standards Selection**

| S1 | S2 | Format | Memory Pages |
|---|---|---|---|
| LMB | NTSC | NTSC | 0-15 |
| LMB | PAL | PAL B/I | 16-31 |
| UMB | NTSC | NTSC-EIA | 32-47 |
| UMB | PAL | PAL-M | 48-63 |

**Table 3. EPROM Address Map**

| Address | Contents |
|---|---|
| 0 | |
| 1 | CLUT address pointer set to 00h |
| 2 | Start of CLUT data |
| : | $V_{n-1}$ |
| : | $V_n$ |
| : | $V_{n+1}$ |
| 769 | End of CLUT data |
| 770 | Control Register pointer set to 00h |
| 771 | Start of Control Register data |
| : | : |
| 851 | End of Control Register data |
| 852 | Unused locations set to 00h |
| : | : |
| 896 | Unused locations set to 00h |
| 897 | Set address pointer to 00h |
| 898 | Start of control register data |
| : | : |
| 930 | End of control register data |
| 931 | Unused locations set to 00h |
| : | : |
| 1023 | Unused locations set to 00h |

## Output Reconstruction Filters

The 2x oversampling of internal digital data before the output D/A converters of the TMC22091 and TMC2490 not only reduces the Sin(x)/x high-frequency roll-off but eliminates complicated reconstruction filters. This is particularly important as the frequency response of digital filters is dependent upon the sample rate, while the frequency of the aliased subcarrier component is fixed. The TMC22091 and TMC2490 encoder are designed to drive a 75 Ω line, terminated both at the source and at the load (that is, a 37.5 Ω load). The filters are internally source terminated. Optional load terminations are provided on the board. If these are not required, simply remove the appropriate links behind the BNC connectors E9, E10, E11, E12, E13, and E14).

## TMC22091 Operation Without a CCIR-601 Source

Only rotary switch positions 0, 1, and 2 are useful without a D1 digital video source available. These switch positions produce color bars and a modulated ramp. These test patterns are inserted into the pixel data path after the CLUTs in RGB format and demonstrate 90% of the circuitry of the TMC22091. To provide a PXCK in the absence of a D1 source, switch E3 to INTernal.

## Power Supply Requirements

The TMC2063P7C board requires 1.5 Amps from the +5 Volt power supply and 0.25 Amps from the -5 Volt power supply. The -5 Volt power supply powers ECL logic devices which have relatively good noise immunity. The +5 Volt power supply not only drives TTL logic devices but it also provides the power to the TMC22091 and TMC2490. Therefore, it is recommended that a bench power supply be used with the cable lengths kept to a minimum. When operating in stand-alone mode, only the +5 Volt supply is required.

**Table 4. TMC2063 Parts List**

| Item | Qty | Part/Value | Ref. Designator | P/N, Mfg. No. |
|---|---|---|---|---|
| 1 | 3 | Ferrite Beads | L1, L2, L3 | 2743001112, FAIR-RITE Product Corporation |
| 2 | 6 | Inductors, 1.8μH | L10 - L15 | IMS-2 1.8μH ±5% Dale |
| 3 | 6 | Inductors, 1.0μH | L4 - L9 | IMS-2 1.0μH ±5% Dale |
| 4 | 43 | Ceramic capacitor, 0.1μF | C4, C5, C9 - C41, C43 - C49, C51 | MD015C104KAB, AVX (C46 and C47 optional) |
| 5 | 4 | Ceramic capacitor, 0.01μF | C3, C6, C42, C50 | MD015C103KAB, AVX |
| 6 | 6 | Ceramic capacitor, 27 pF | C65, C67, C69, C71, C73, C75 | SR151A270JAA, AVX |
| 7 | 6 | Ceramic capacitor, 100 pF | C52, C54, C56, C58, C60, C62 | SR151A101JAA, AVX |
| 8 | 12 | Ceramic capacitor, 330 pF | C53, C55, C57, C59, C61, C63, C64, C66, C68, C70, C74, C74 | SR151A331JAA, AVX |
| 9 | 2 | Tantalum capacitor, 0.47μF | C7, C8 | TAP474K035SCS, AVX |
| 10 | 2 | Tantalum capacitor, 22 | C1, C2 | TAP226K035HSB, AVX |
| 11 | 18 | Resistor, 75Ω | R29-R46 | RN50C75R0F |
| 12 | 9 | Resistor, 121Ω | R1-R5, R9 - R12 | RN50C1210F |
| 13 | 2 | Resistor, 475Ω | R23, R24 | RN50C4750F |
| 14 | 2 | Resistor, 3.32kΩ | R19, R22 | RN50C3321F (optional) |
| 15 | 8 | Resistor, 4.75kΩ | R6, R7, R13, R14, R17, R18, R20, R21 | RN50C4751F |
| 16 | 1 | Resistor, 47.5kΩ | R8 | RN50C4752F |
| 17 | 1 | SIP resistor, 3.3kΩ | RN2 | 4308R-101-332, Bourns |
| 18 | 1 | SIP resistor, 3.3kΩ | RN1 | 4310R-101-332, Bourns |
| 19 | 2 | Variable resistor, 5kΩ | R27, R28 | RJ26FW502, MEPCOPAL |
| 20 | 1 | Resistor, 1Ω, .25W | R15 | R25XT68J1R0 |
| 21 | 1 | Resistor, 10kΩ | R16 | RN50C1002F |
| 22 | 2 | Resistor, 750 Ω | R25, R26 | RN50C7500F |
| 23 | 1 | 1N4148 Silicon Diode | CR5 | 1N4148 |
| 24 | 2 | LT1004 Bandgap Reference | CR7, CR8 | LT1004-1.2, Linear Technology (optional) |
| 25 | 2 | 1N4004 Silicon Diode | CR3, CR4 | 1N4004, Motorola |
| 26 | 1 | Orange LED | CR2 | 550-0806, DIALIGHT |
| 27 | 2 | Red LED | CR1, CR6 | 550-0506, DIALIGHT |
| 28 | 12 | 1N5818 Silicon Diode | CR9 - CR20 | 1N5818 |
| 29 | 1 | TMC22091 Encoder | U28 | TMC22091R0C, Fairchild |
| 30 | 1 | TMC2490 Encoder | U29 | TMC2490R0C, Fairchild |
| 31 | 2 | 16R8 PAL | U8, U13 | TIBPAL16R8-15CN, Texas Instruments |
| 32 | 2 | 20R8 PAL | U15, U16 | TIBPAL20R8-15CNT, Texas Instruments |
| 33 | 1 | 20R4 PAL | U18 | TIBPAL20R4-15CNT, Texas Instruments |
| 34 | 1 | 27512 EPROM | U22 | TMS27C512-120JL, Texas Instruments |

**Table 4. TMC2063 Parts List** (continued)

| Item | Qty | Part/Value | Ref. Designator | P/N, Mfg. No. |
|---|---|---|---|---|
| 35 | 3 | 10125 ECL-TTL Translator | U2 - U4 | MC10125P, Motorola |
| 36 | 1 | 74LS04 Hex Inverter | U25 | SN74LS04N, Texas Instruments or equivalent |
| 37 | 1 | 74F08 Quad 2-input AND | U1 | MC74F08N, Motorola or equivalent |
| 38 | 1 | 74LS74 Dual D-type FF | U9 | MC74LS74AN, Motorola or equivalent |
| 39 | 3 | 74F163 4-bit counter | U6, U7, U12 | MC74F163AN, Motorola or equivalent |
| 40 | 3 | 74LS163 4-bit counter | U5, U10, U11 | MC74LS163AN, Motorola or equivalent |
| 41 | 1 | 74F174 Hex D-type FF | U17 | MC74F174AN, Motorola or equivalent |
| 42 | 2 | 74LS244 Octal Buffer | U26, U27 | SN74LS244N, Texas Instruments or equivalent |
| 43 | 2 | 74F374 Octal D-type FF | U14, U19 | MC74F374N, Motorola or equivalent |
| 44 | 2 | 74HCT374 Octal D-type | U23, U24 | MC74HCT374N, Motorola or equivalent |
| 45 | 2 | 74F377 Octal D-type FF | U20, U21 | MC74F377N, Motorola or equivalent |
| 46 | 1 | Crystal oscillator | Y1 | MXO-55GA-2C-27MHz, CTS-Knight or F1100H-27MHz, Fox |
| 47 | 21 | Test points | TP1 - TP21 | ME151-203-1000, Mouser |
| 48 | 11 | Shorting block | | ME151-8000, Mouser |
| 49 | 1 | 26 Pin Dual Header | JP1 | NSH-26DB-S1-TR, Robinson-Nugent |
| 50 | 1 | 48 Pin Dual Header | JP2 | NSH-48DB-S1-TR, Robinson-Nugent (optional) |
| 51 | 1 | 60 Pin Dual Header | JP3 | NSH-60DB-S1-TR, Robinson-Nugent (optional) |
| 52 | 8 | Jumpers | E1, E9 - E14, E15 | NSH-02SB-S1-TR, Robinson-Nugent |
| 53 | 1 | Power Connector | J1 | ELM033100, PCD |
| 54 | 6 | BNC connectors | J3 - J5, J7 - J9 | 31-5431, Amphenol |
| 55 | 2 | S-VIDEO Connector | J2, J6 | 749263-1, Amphenol |
| 56 | 1 | 25-pin D-connector | P1 | 617UO25SAJ220, Amphenol |
| 57 | 1 | ACCESS BUS connector | P2 | 15-83-0064, Molex |
| 58 | 7 | SPDT switch | E2 - E8 | 090320102, Secma Inc. |
| 59 | 1 | SPDT switch | S3 | ATIDG-RA-1, Alco Switch |
| 60 | 1 | SPDT Push button switch | S2 | TP11FG-RA-0, Alco Switch |
| 61 | 1 | HEX rotary switch | S1 | 350134GSV, EECO |
| 62 | 1 | 84 pin PLCC socket | U28 | PLCCB-84-PS-T, Robinson-Nugent |
| 63 | 1 | 44 pin PLCC socket | U29 | PLCCB-44-PS-T, Robinson-Nugent |

**Table 4. TMC2063 Parts List** (continued)

| Item | Qty | Part/Value | Ref. Designator | P/N, Mfg. No. |
|---|---|---|---|---|
| 64 | 1 | 14 pin Oscillator socket | Y1 | ICA-143-SCO-TG30, Robinson-Nugent |
| 65 | 2 | 20-pin DIP socket | U8, U13 | ICA-203-S-TG30, Robinson-Nugent |
| 66 | 3 | 24-pin DIP socket | U15, U16, U18 | ICA-243-S-TG30, Robinson-Nugent |
| 67 | 1 | 28-pin DIP socket | U22 | ICA-286-S-TG30, Robinson-Nugent |
| 68 | 2 | Universal transistor mount | CR7, CR8 | 111-080, BIVAR (optional) |
| 69 | 5 | 4-40 3/8” Pan Head, Phillips Screws | | Western Fastener |
| 70 | 5 | Standoff | | 1902F, Keystone |
| 71 | 1 | Bare PC Board | | 40X07572 Rev. B, Fairchild |

## PAL Functions Listings

Following are the programmable array logic listings of the devices used on the TMC2063P7C evaluation board. These listings are shown as ABEL_HDL source files. The following brief tutorial refers only to terms used for programming logic used on this board.

### Sets

A set is a collection of signals and constants that are operated on as one unit. Any operation applied to a set is applied to each element in the set. For example, in U9,

count = [c3,c2,c1,c0]

### Valid operations used in the TMC2063:

| Operator | Example | Description |
|---|---|---|
| := | A := [1,0,1] | registered assignment |
| ! | !A | NOT: ones complement |
| & | A & B | AND |
| # | A # B | OR |
| == | A == B | equal |
| != | A != B | not equal |
| < | A < B | less than |
| <= | A <= B | less than or equal |
| > | A > B | greater than |
| >= | A >= B | greater than or equal |

### The Basic Elements Of A Source File

**Module** The module statement names the module and indicates the presence of any dummy variables used.

**Title** The title statement can be used to give a title or description for the module.

**Declarations** Declarations associate names with devices, pins, nodes, constants, macros, and sets.

**Equations** It is possible to use equations, state diagrams, or truth tables to describe logic designs. All programmable devices use equations.

**End** The end statement terminates the module. Comments begin with double quotation marks, " ", and end with either another double quotation mark or the end of line, whichever comes first.

## Code Segment 1. U8 – VVSYNC and Reset Logic

```
Board Reference Designator U8
Module bd3_u8
Title 'VVSYNC generation and reset control logic'
Declarations
       bd3_u8 device 'P16R8';
"inputs"
       clk,v,pn,f                  pin 1,2,3,4;
       s_reset                     pin 7;
"outputs"
       c0,c1,c2,c3                 pin 19,18,17,16;
       fb,vvsync,pgmfb,pgm         pin 15,14,13,12;
"notation"
       count = [c3,c2,c1,c0];
       t = (s reset & !pgmfb) # pgm # (v & s_reset & !pgm & pgmfb);
Equations
       !c0        := c0 & t & (count != 15)
                  #  !t;
       !c1        := !c0 & !c1 & t & (count != 15)
                  #  c0 & c1 & t (count != 15)
                  #  !t;
       !c2        := !c2 & !c0 & t & (count != 15)
                  #  !c2 & !c1 & t & (count != 15)
                  #  c2 & c1 & c0 & t & (count != 15)
                  #  !t;
       !c3        := !c3 & !c0 & t & (count != 15)
                  #  !c3 & !c1 & t & (count != 15)
                  #  !c3 & !c2 & t & (count != 15)
                  #  !t;
       !vvsync    := !fb & pn & ((count >= 3) & (count <= 5))
                  #  fb & ((count >= 4) & (count <= 5))
                  #  !fb & !pn & (count == 5)
                  #  ((count >= 6) & (count <= 7));
       !fb        := (!fb & v) # (f & !v);
       pgmfb      := s_reset;
       !pgm       := (count == 15)
                  #  s_reset & pgmfb & !pgm
                  #  !s_reset;
End    bd3_u8
```

## Code Segment 2. U15 – TMC22091 Programming Control

```
Board Reference Designator U15
Module  bd3_u15
Title   'TMC22091 programming control'
Declarations
       bd3_u15 device "P20R8';
"inputs"
       clk                          pin 1;
       a0,a1,a2,a3,a4,a5,a6         pin 2,3,4,5,6,7,8;
       a7,a8,a9,a10,a11             pin 9,10,11,14,23;
"outputs"
       offset,zero,countclr         pin 22,21,20;
       dck,rw,cs,aa1,aa0            pin 19,18,17,16,15;
"notation"
       addr = [a11..a0];
Equations
       !offset    := ((addr >= 3081) & (addr < 3265));
       !zero      := (addr == 0)
                  #  ((addr >= 3264) & (addr <= 3327));
       countclr:= (addr >= 3836);
       !dck       := !a1 & a11
                  #  !a1 & !rw;
       !rw        := zero & (addr <= 3261);
       !cs        := (a1 & a0)
                  #  (!a1 & !a0)
                  #  (addr >= 3263)
                  #  !zero;
       !aa1       := (addr <= 9)
                  #  ((addr >= 3082) & (addr <= 3085))
                  #  !zero;
       !aa0       := !offset
                  #  (addr >= 3264)
                  #  !zero;

End    bd3_u15
```

## Code Segment 3. U19 – VHSYNC and Data Control Logic

```
Board Reference Designator U19
Module  bd3_u19
Title 'VHSYNC generation and data control logic'
Declarations
       bd3_u19 device 'P20R8';
"inputs"
       a0,a1,a2,a3,a4,a5,a6          pin 2,3,4,5,6,7,8
       a7,a8,a9,a0                   pin 9,10,11,14;
       clk,pn                        pin 1,23;
"outputs"
       vhsync,hclk                   pin 22,20;
       h2clk,den,pclk                pin 19,18,17;
       fb                            pin 16;
"notation"
       addr = [a10..a0];
Equations
       !vhsync    := ((addr >= 16) & (addr <= 256));
       !hclk      := ((addr >= 1712) & (addr <= 16));
       h2clk      := ((addr >= 15) & (addr < 256))
                  # !fb;
       !den       := a0;
       !pclk      := !a0;
       !fb        := ((addr >=766) & (addr < 1015);

End bd3_u19
```

## Code Segment 4. U13 – TRS Decode

```
Board Reference Designator U13
Module  bd3_u13
Title   'TRS decode'
Declarations
       bd3_u13 device 'P16R8';
"inputs"
       d0,d1,d2,d3,d4,d5,d6,d7      pin 2,3,4,5,6,7,8,9;
"outputs"
       p1,p2,p3,f,v,h               pin 19,18,17,16,15,14;
       p_reset,ldvpin 13,12;
"notation"
       data = [d7..d0];
Equations
       !p1         := (data == ^hFF);
       !p2         := (data == ^h00) & !p1;
       !p3         := (data == ^h00) & !p2;
       !h          := (!h & p3) # (!d4 & !p3);
       !v          := (!v & p3) # (!d5 & !p3 & !d4)
                   #  (!v & !p3 & d4);
       !f          := (!f & p3) # (!d6 & !p3 & !d4)
                   #  (!f & !p3 & d4);
       !p_reset    := !p3 & d4;
       !ldv        := !p_reset # ldv;

End    bd3_u13
```

## Code Segment 5. U16 – TMC2490 Programming Control

```
Board Reference Designator U16
Module bd3_u16
Title 'TMC22091 programming control'
Declarations
       bd3_u16 device 'P20R4';
"inputs"
       clk                          pin 1;
       a0,a1,a2,a3,a4,a5,a6         pin 2,3,4,5,6,7,8;
       a7,a8,a9,a10,a11             pin 9,10,11,14,23;
       ser,setsa0                   pin 22,15;
"outputs"
       poe,rw,cs,fb1,fb2,adr        pin 21,20,19,18,17,16;
"notation"
       addr = [a11..a0];

Equations
       poe        =  !ser;
       !rw        := (addr >= 3588);
       !cs        := (a1 & a0)
                  #  (!a1 & !a0)
                  #  fb1
                  #  (addr == 0);
       !adr       =  !setsa0 & !ser
                  #  !fb2;
       fb1        := (addr < 3588);
       fb2        := ((addr >= 3594) & (addr <= 3730));

End bd3_u16
```

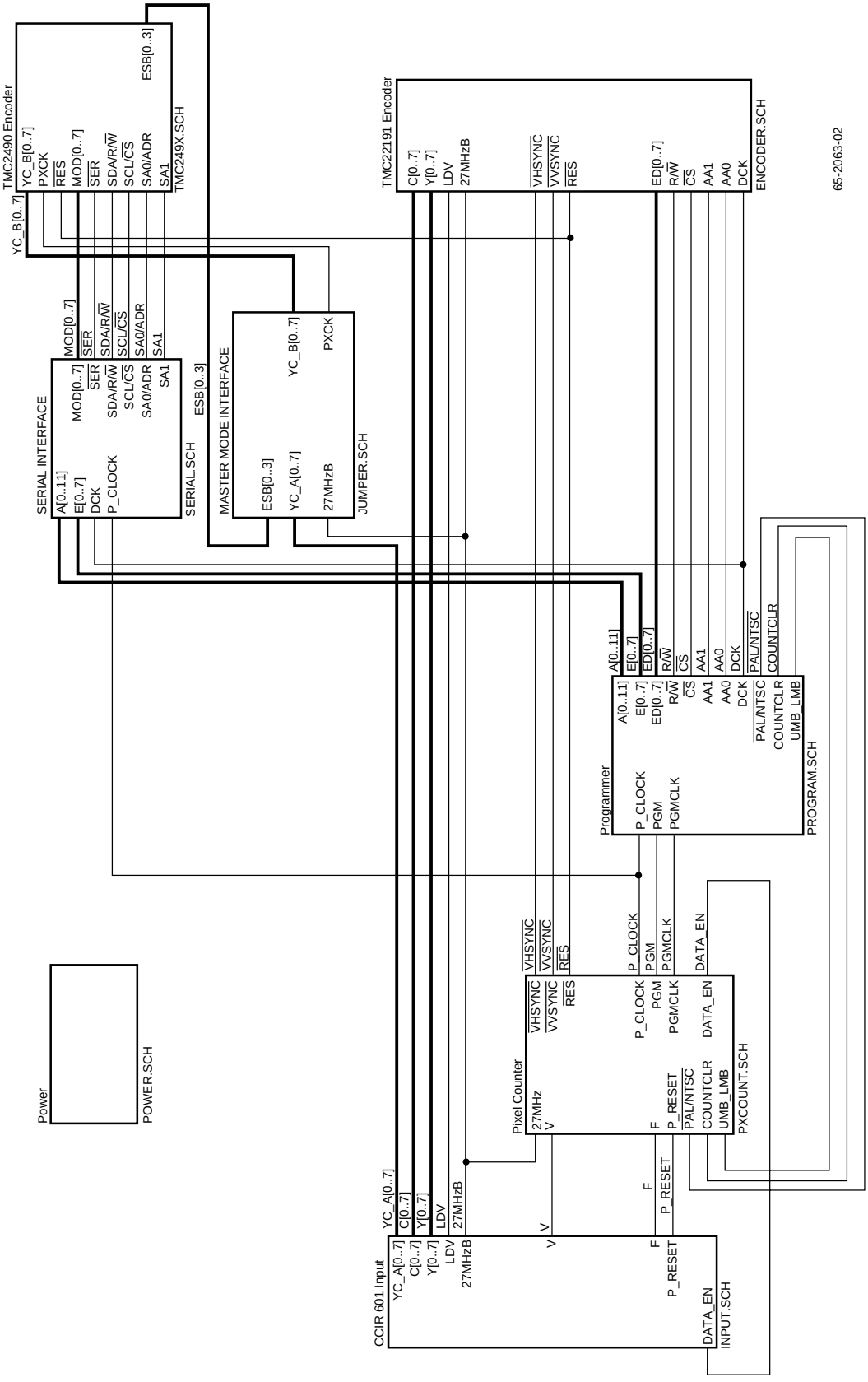



**Figure 1. Digital Video Encoder Demonstration Board**

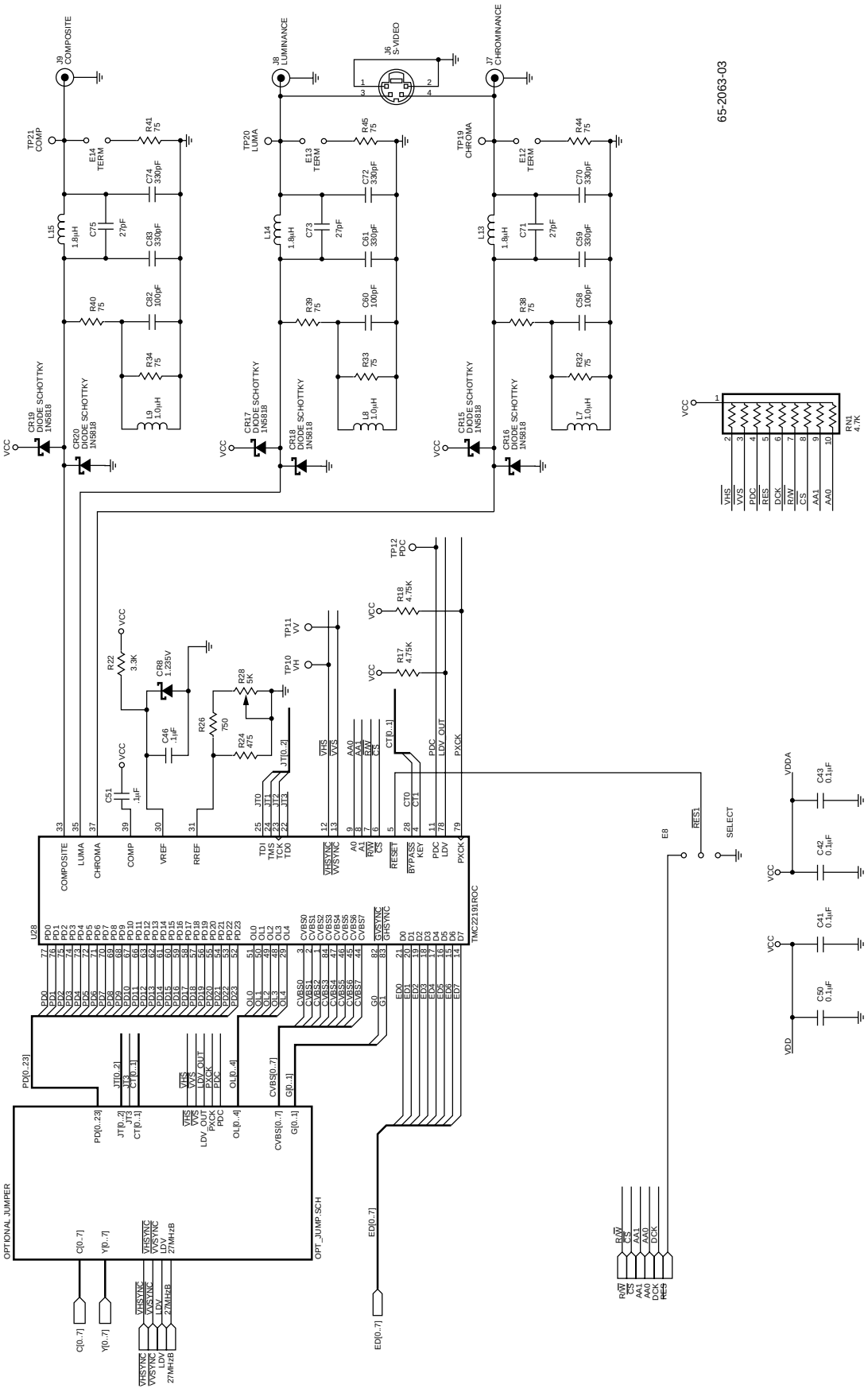



**Figure2. Digital Video Encoder Demonstration Board**

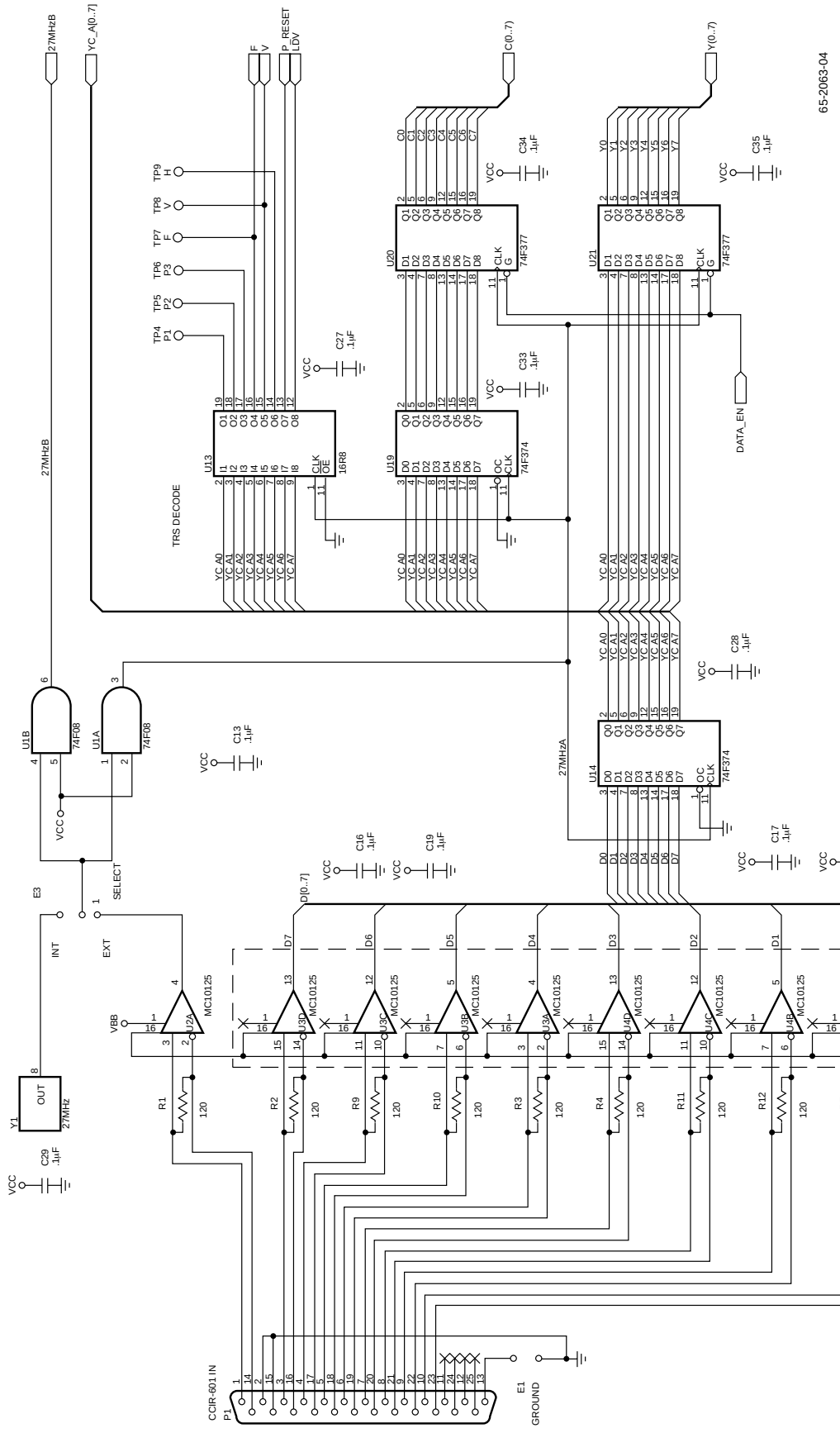



**Figure 3. Digital Video Encoder Demonstration Board**

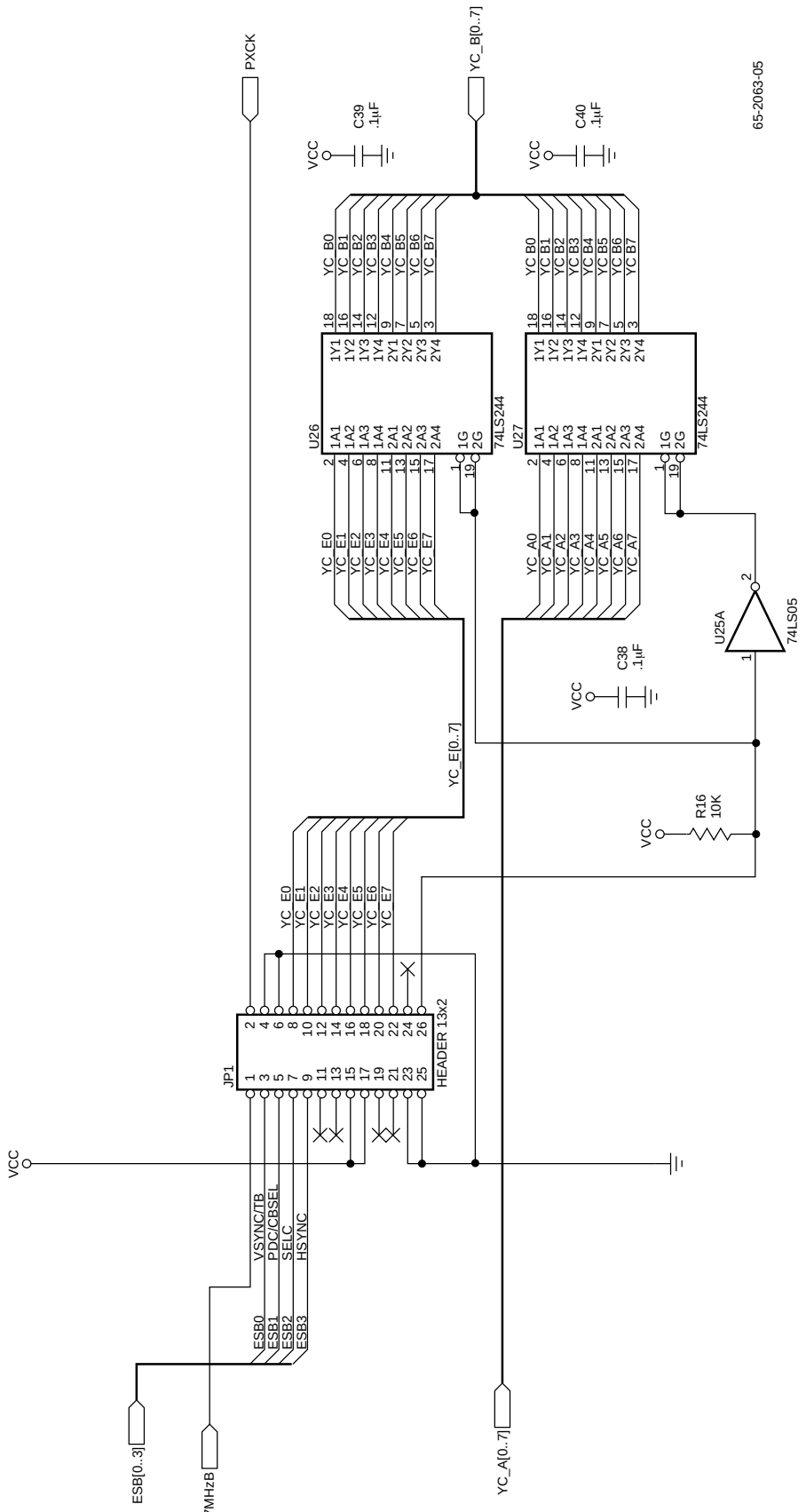



**Figure 4. Digital Video Encoder Demonstration Board**

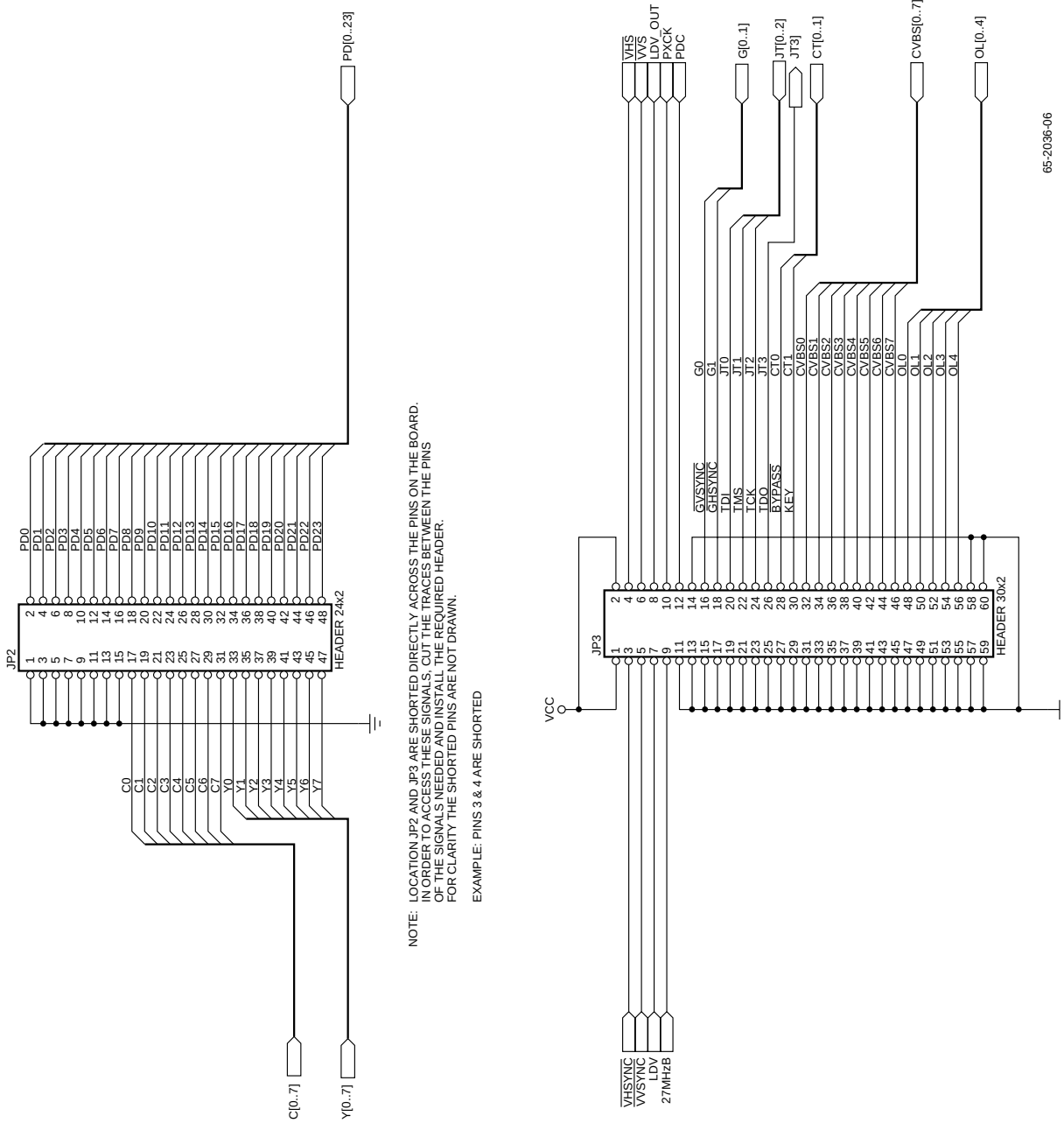



**Figure 5. Digital Video Encoder Demonstration Board**

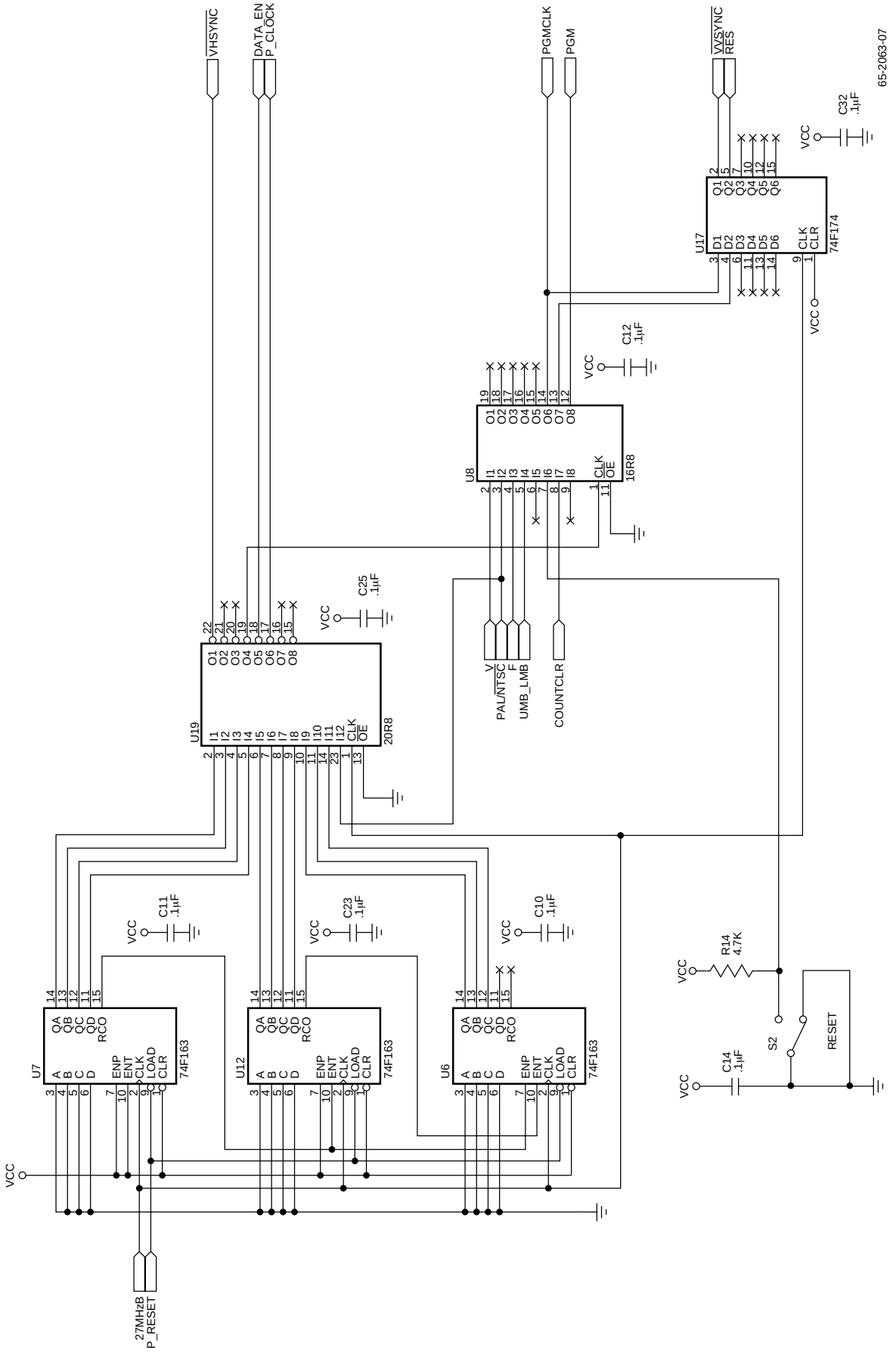



**Figure 6. Digital Video Encoder Demonstration Board**

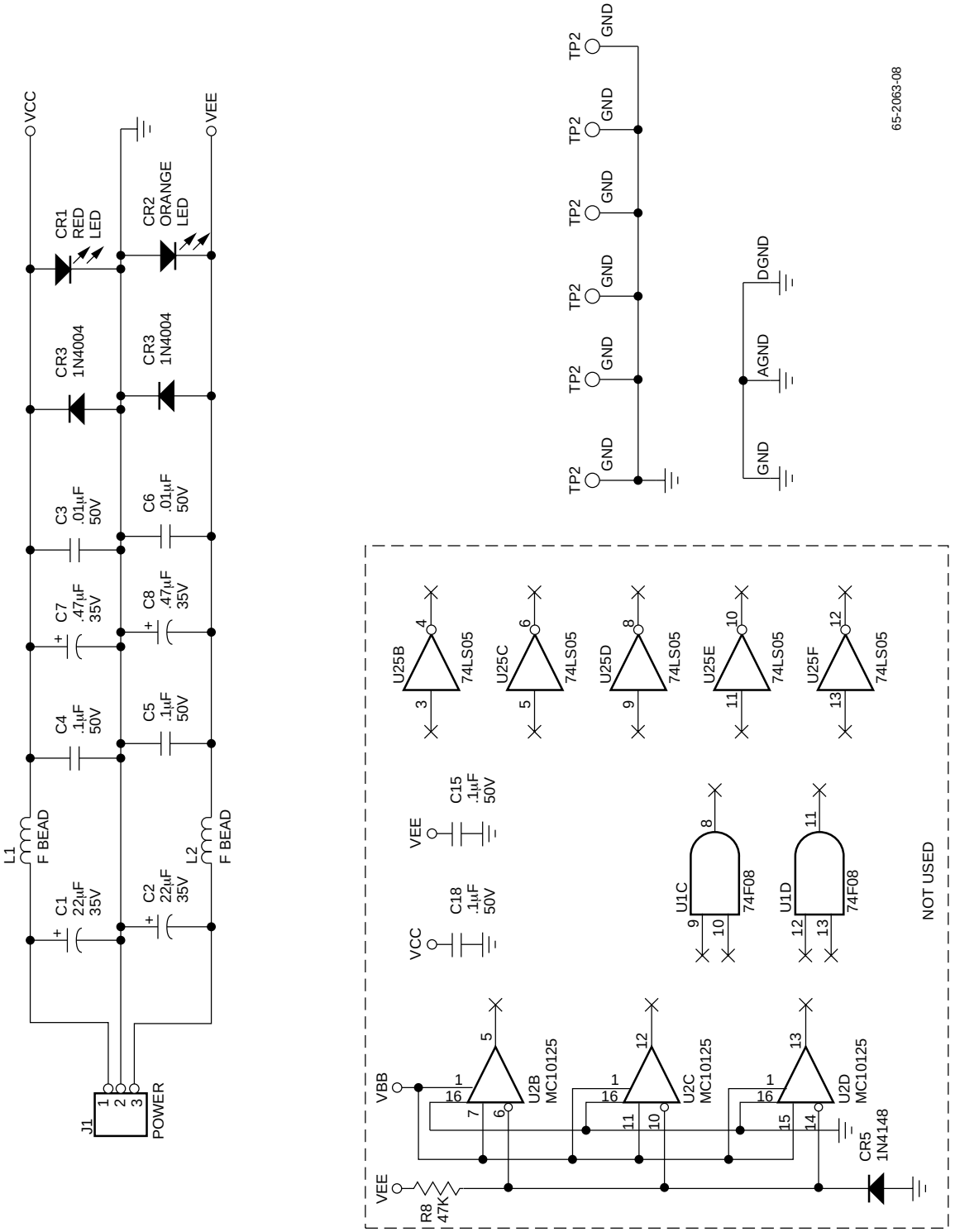



**Figure 7. Digital Video Encoder Demonstration Board**

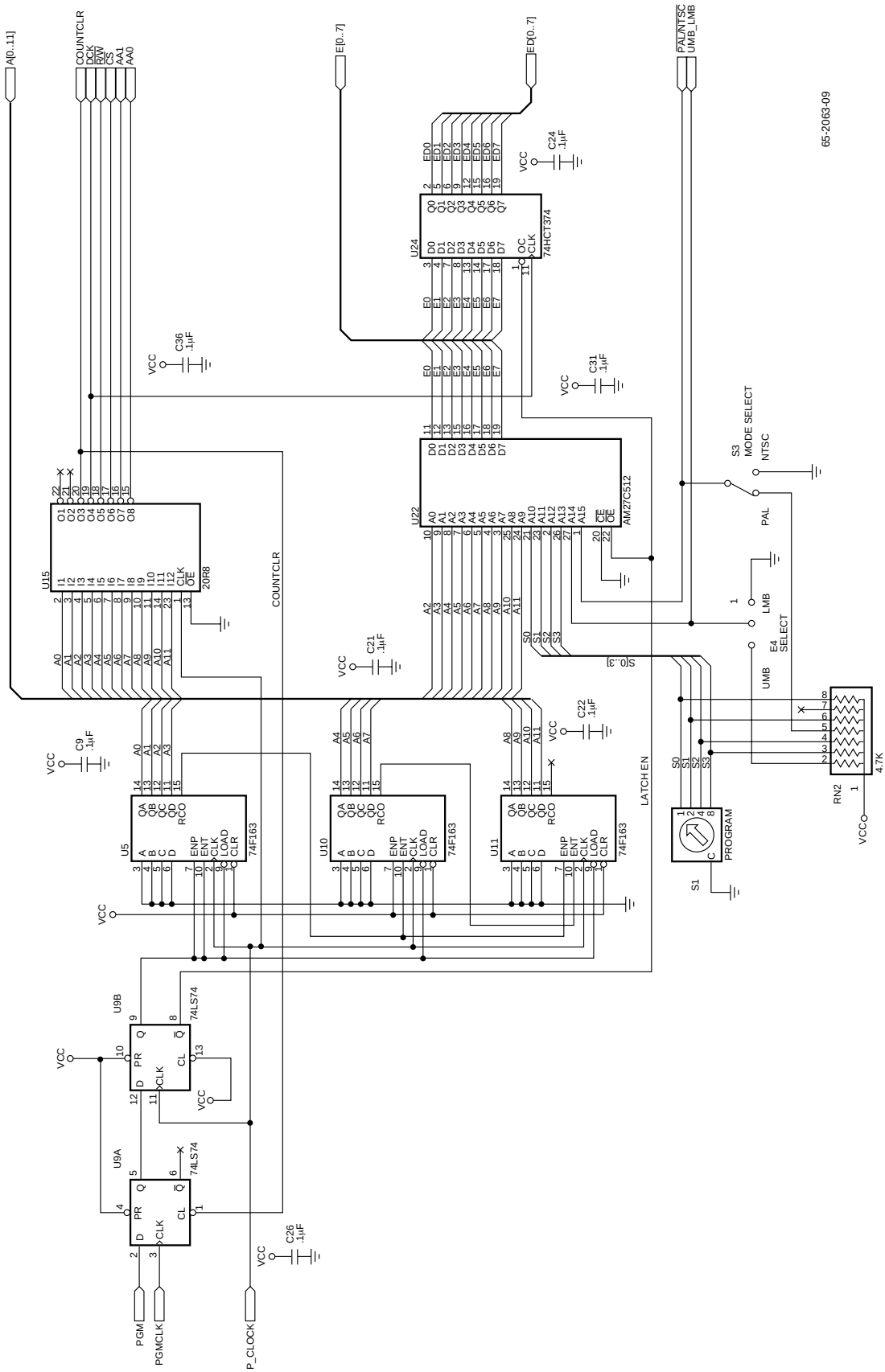



**Figure 8. Digital Video Encoder Demonstration Board**

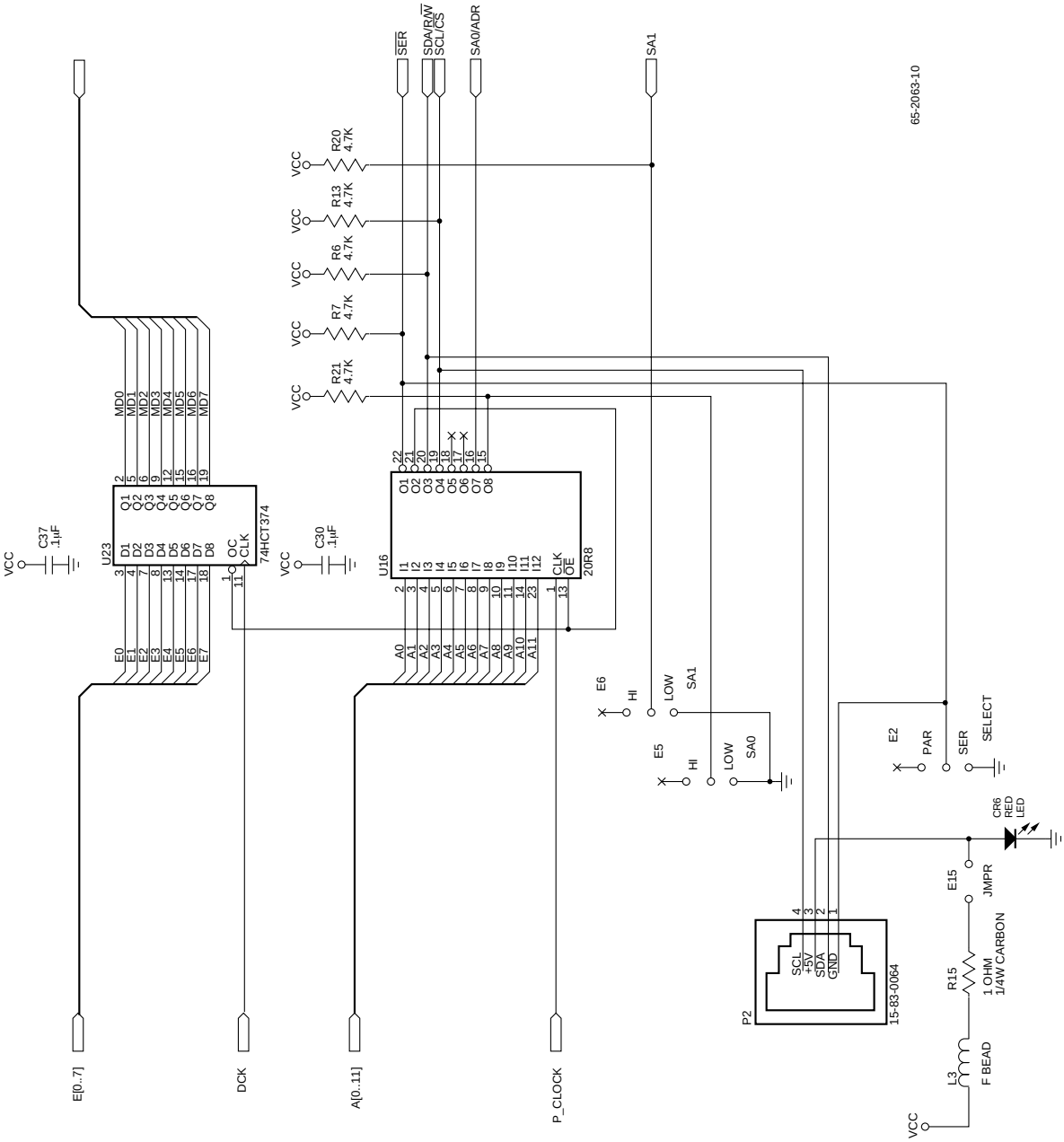



**Figure 9. Digital Video Encoder Demonstration Board**

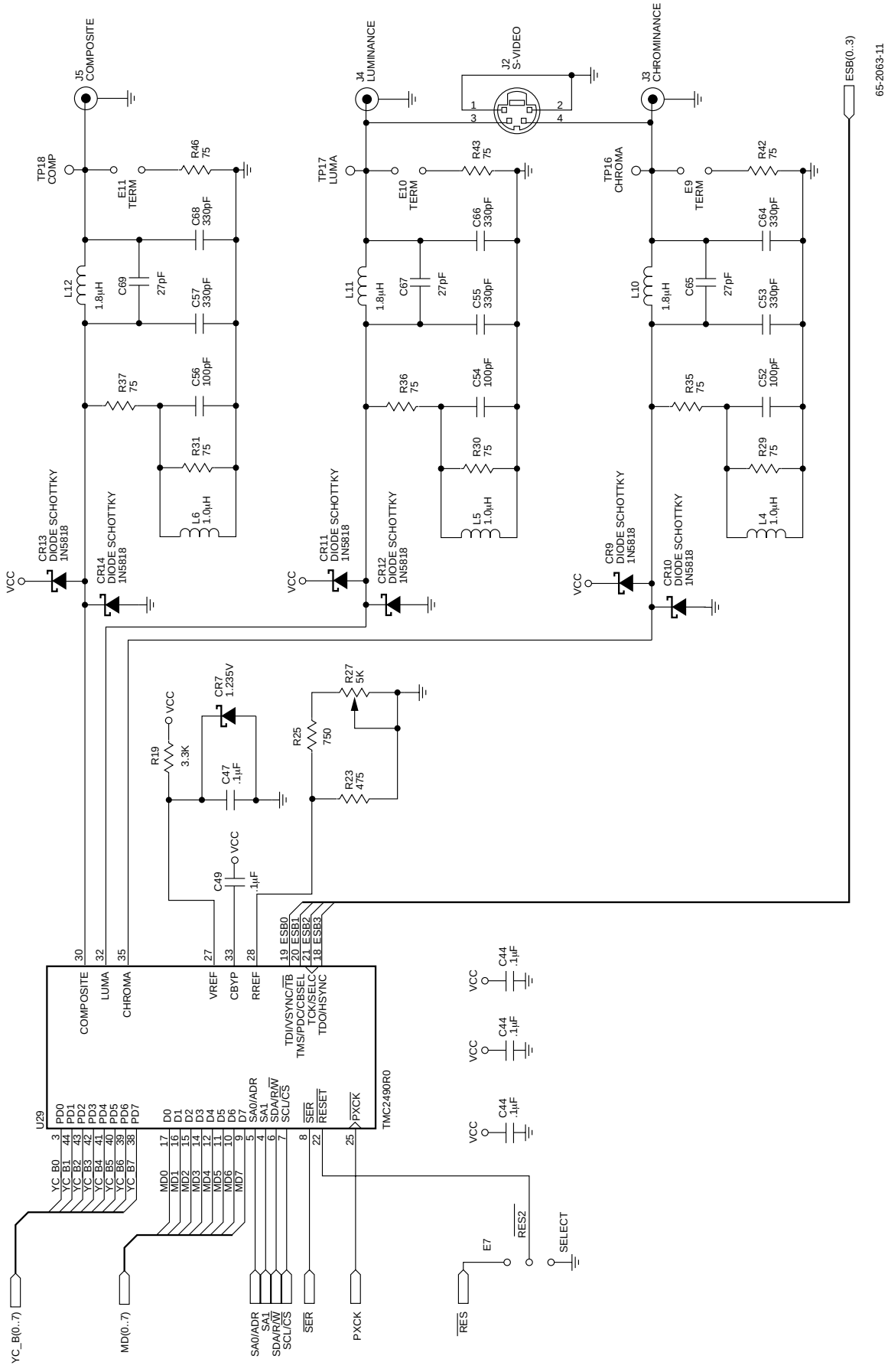



**Figure 10. Digital Video Encoder Demonstration Board**

## Related Products

- TMC22191 Digital Video Encoder
- TMC2490 Digital Video Encoders

# Ordering Information

| Product Number | Temperature Range | Speed Grade | Screening | Package | Package Marking |
|---|---|---|---|---|---|
| TMC2063P7C | 25˚C | 27 MHz | Commercial | 6" by 9" Printed Circuit Board | TMC2063P7C |

A schematic database is available in OrCAD™ format, along with PAL and EPROM maps. Contact the factory.

The TMC2063 Demonstration Board, design documentation, and software are provided as a design example for the customers of Fairchild. Fairchild makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

All parameters contained in this specification are guaranteed by design, characterization, sample testing or 100% testing as appropriate. Fairchild reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of Fairchild Company or others.

## FCC Compliance

This device has not been approved by the Federal Communications Commission (FCC). This device is not and may not be offered for sale or lease or sold or leased until the approval of the FCC has been obtained.